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			2.	A 150-MOPS GaAs 8-bit slice processor Gauthier, R.V.; Weissman, J.; Peterson, B.E.; Florez, J.M.; Solid-State Circuits, IEEE Journal of Volume 23, Issue 5, Oct. 1988 Page(s):1195 - 1202		
				AbstractPlus Full Text: PDE(612 KB) WEST UNIX.		
			3.	An efficient technique for exploring register file size in ASIP design Jain, M.K.; Balakrishnan, M.; Kumar, A.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 23, Issue 12, Dec. 2004 Page(s):1693 - 1699		
				AbstractPlus References Full Text: PDF(304 KB) IEEE JPN.		
			4.	A 130-nm 6-GHz 256 × 32 bit leakage-tolerant register file Krishnamurthy, R.K.; Alvandpour, A.; Balamurugan, G.; Shanbhag, N.R.; Soumyanath, K.; Borkar, S.Y.; Solid-State Circuits, IEEE Journal of Volume 37, Issue 5, May 2002 Page(s):624 - 632		
				AbstractPlus References Full Text: PDE(319 KB)		
			5.	Analysis of the influence of register file size on energy consumption, code size, and execution time Wehmeyer, L.; Jain, M.K.; Steinke, S.; Marwedel, P.; Balakrishnan, M.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 20, Issue 11, Nov. 2001 Page(s):1329 - 1337		
				AbstractPlus References Full Text: PDF(320 KB) INSECTION STATE AND ADDRESS		
			6.	A 2-GHz clocked AlGaAs/GaAs HBT byte-slice datapath chip Carlough, S.R.; Philhower, R.A.; Maier, C.A.; Steidl, S.A.; Campbell, P.M.; Garg, A.; Kyung-Suc Nah; Ernest, Krawczyk, T.W., Jr.; Curran, P.F.; Kraft, R.P.; Greub, H.J.; McDonald, J.F.; Solid-State Circuits, IEEE Journal of Volume 35, Issue 6, June 2000 Page(s):885 - 894		
				AbstractPlus References Full Text: PDF(748 KB)		

7.	A 500-MHz, 32-word×64-bit, elght-port self-resetting CMOS register file Wei Hwang; Joshi, R.V.; Henkels, W.H.; Solid-State Circuits, IEEE Journal of Volume 34, Issue 1, Jan. 1999 Page(s):56 - 67
	AbstractPlus References Full Text: PDE(412 KB) IEEE JNL
8.	Nonscan design-for-testability techniques using RT-level design information Dey, S.; Potkonjak, M.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 16, Issue 12, Dec. 1997 Page(s):1488 - 1506
	AbstractPlus References Full Text: PDF(340 KB) IEEE JNL
9.	Datapath synthesis using onchip multiport memories Ahmad, I.; Chen, C.Y.R.; Computers and Digital Techniques, IEE Proceedings- Volume 140, Issue 4, Jul 1993 Page(s):227 - 232
	AbstraciPlus Full Text: PDE(388 KB) IEE JNL
10	. The energy complexity of register files Zyuban, V.; Kogge, P.; Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on 10-12 Aug 1998 Page(s):305 - 310
	AbstractPlus Full Text: PQF(688 KB) IEEE CNF
11.	A GaAs 32-bit RISC microprocessor Harrington, D.L.; Troeger, G.L.; Gee, W.C.; Bolen, J.A.; Vogelsang, C.H.; Nicalek, T.P.; Lowe, C.M.; Roh, Y.k J.F.; Reeder, J.; Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1988. Technical Digest 1988., 10th Annual IEEE 6-9 Nov. 1988 Page(s):87 - 90
	AbstractPlus Full Text: PDE(248 KB) IEEE CNF
12.	Interconnect optimisation during data path allocation Stok, L.; Design Automation Conference, 1990. EDAC. Proceedings of the European 12-15 March 1990 Page(s):141 - 145
	AbstractPlus Full Text: PDE(396 KB) #문문문 CNF
13.	A heuristic for data path synthesis using multiport memories Ahmad, I.; Chen, C.Y.R.; VLSI, 1992., Proceedings of the Second Great Lakes Symposium on 28-29 Feb. 1992 Page(s):44 - 51
	AbstractPlus Full Text: PDF(564 KB) IEEE CNF
14.	An environment for evaluating architectures for spatially mapped computation: System architecture a Herbordt, M.C.; Weems, C.C.; Computer Architectures for Machine Perception, 1993. Proceedings 15-17 Dec. 1993 Page(s):191 - 201
	AbstractPlus Full Text: PDF(760 KB) IEEE CNF
15.	Synthesis of memories from behavioral HDLs Vander Zanden, N.; ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International 19-23 Sept. 1994 Page(s):71 - 74
	AbstractPlus Full Text: PDF(260 KB) IEEE CNF
16.	Multithreaded vector architectures

		Espasa, R.; Valero, M.; High-Performance Computer Architecture, 1997., Third International Symposium on 1-5 Feb. 1997 Page(s):237 - 248
		AbstractPlus Full Text: PDF(1248 KB) RESERVED CNE
	17.	A graph-theoretic approach for register file based synthesis Ravikumar, C.P.; Aggarwal, R.; Sharma, C.; VLSI Design, 1997. Proceedings., Tenth International Conference on 4-7 Jan. 1997 Page(s):118 - 123
		AbstractPlus Full Text: PDF (500 KB) → NESSE CAPE
	18.	An eight-issue tree-VLIW processor for dynamic binary translation Ebcioglu, K.; Fritts, J.; Kosonocky, S.; Gschwind, M.; Altman, E.; Kailas, K.; Bright, T.; Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conferent 5-7 Oct. 1998 Page(s):488 - 495
		AbstractPlus Full Text: PDF(108 KB) KHIEL CNF
	19.	Teaching computer architecture/organisation using simulators Grunbacher, H.;
		Frontiers in Education Conference, 1998. FIE '98. 28th Annual Volume 3, 4-7 Nov. 1998 Page(s):1107 - 1112 vol.3
		AbstractPlus Full Text: PDF(1664 KB) NEW CNIF
	20.	A 690 ps read-access latency register file for a GHz integer microprocessor Takahashi, O.; Silberman, J.; Dhong, S.; Hofstee, P.; Aoki, N.; Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings., International Conferent 5-7 Oct. 1998 Page(s):6 - 10
		AbstractPlus Full Text: PDF(820 KB) IEIIE CN#
	21.	Automated design of wave pipelined multiport register files Takano, K.; Sasaki, T.; Oba, N.; Kobayashi, H.; Nakamura, T.; Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific 10-13 Feb. 1998 Page(s):197 - 202
		AbstractPlus Full Text: PDF(548 KB) → NESSH CANF
	22.	Memory design and exploration for low power, embedded systems Wen-Tsong Shiue; Chakrabarti, C.; Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop on
		20-22 Oct. 1999 Page(s):281 - 290
		AbstractPlus Full Text: PDF(508 KB) REHRE CNF
.	23.	A 0.29 ns 32-word by 32 b three-port bipolar register file implemented using a SiGe HBT BICMOS tech Steidl, S.A.; McDonald, J.F.; Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International
		15-17 Feb. 1999 Page(s):194 - 195
•		AbstractPlus Full Text: PDF(236 KB) NEEE 다양
	24.	Determining the optimum extended instruction-set architecture for application specific reconfigurable Alippi, C.; Fornaciari, W.; Pozzi, L.; Sami, M.;
		Rapid System Prototyping, 12th International Workshop on, 2001. 25-27 June 2001 Page(s):50 - 56
		AbstractPlus Full Text: PDF(596 KB) KHIER CNF
	25.	Exploiting loop-level parallelism with the Shift Architecture
		Lima, C.D.; Nakamura, T.; Computer Architecture and High Performance Computing, 2002. Proceedings. 14th Symposium on 28-30 Oct. 2002 Page(s):184 - 191

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				AbstractPlus	Full Text: PDF(764 KB)	HEERE CAP	
				Anders, M.; M VLSI Circuits, 17-19 June 20	SHz 500Mbps 40mW Vite lathew, S.; Krishnamurthy 2004. Digest of Technica 004 Page(s):174 - 175 Full Text: PDE(288 KB)	/, R.; Borkar, S.; al Papers. 2004 Symposi	
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